3 V/5 V Digital Audio Receiver, External APLL

AD1895

FEATURES

CP-1201, CP-340, IEC-958, AES/EBU, S/PDIF Digital Audio Receiver
Status Pins for Stand-Alone Operation
Requires External Analog Phase Lock Loop
Single +3 V to 5 V Supply
Complete Error Reporting
Low Operating Power Dissipation
Three-Wire Serial Data Port with I^2S-Compatible Output Mode
28-Lead SSOP Package

APPLICATIONS

Consumer and Professional Digital Audio Equipment
Computer Multimedia Products

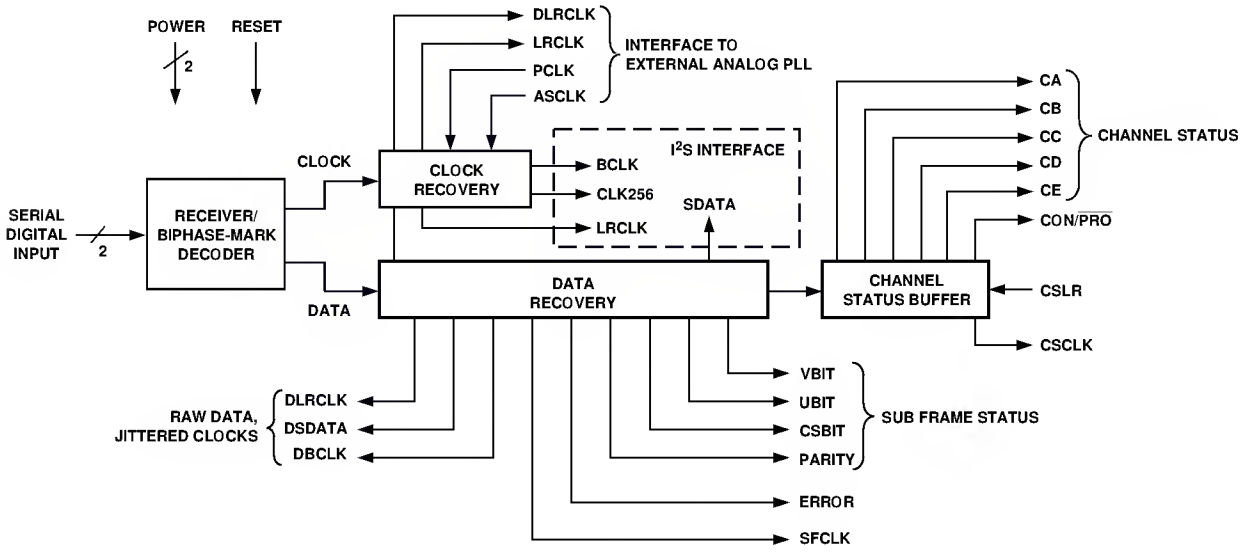
PRODUCT OVERVIEW

The 3 V to 5 V AD1895 is a CP-1201, CP-340, IEC-958, AES/EBU, S/PDIF compatible digital audio receiver (DAR). Key status information from the input digital data stream and the channel status register is reported on output pins on the AD1895, so that the AD1895 may be used in systems which do not include a microcontroller.

The AD1895 uses a proprietary method to lock to the incoming serial digital stream which is superior to other IC implementations. The AD1895 requires an external analog phase lock loop circuit, such as the Texas Instruments TLC2932.

The AD1895 is offered in a 28-pin shrink small outline package (SSOP). It operates over the commercial temperature range from 0°C to +70°C, at a supply voltage from 2.7 V to 5.5 V. Power dissipation at 3 V is TBD. The AD1895 is fabricated in a 0.5 μm single poly, double metal CMOS process.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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AD1895–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltage	+3.0	V
Ambient Temperature	25	°C
Sample Frequency (F_S)	44.1	kHz
Load Capacitance	100	pF

All minimums and maximums tested except as noted.

PERFORMANCE† (Guaranteed for V_{DD} = +3.0 V to +5.0 V ± 10%)

	Min	Max	Units
Interchannel Phase Deviation		0	Degrees
Input Clock Jitter Rejection	10		ns

DIGITAL I/O (Guaranteed for V_{DD} = +3.0 V to +5.0 V ± 10%)

	Min	Max	Units
V_{IH}	2.0		V
V_{IL}		0.8	V
I_{IH} @ V_{IH} = +5.0 V		4	µA
I_{IL} @ V_{IL} = 0 V		4	µA
V_{OH} @ I_{OH} = –4 mA	2.4		V
V_{OL} @ I_{OL} = 4 mA		0.4	V
Input Capacitance†		15	pF

DIGITAL TIMING
(Guaranteed over 0°C to +70°C, V_{DD} = +3.0 V to +5.0 V ± 10%)

		Min	Max	Units
t_{RPWL}	RESET LO Pulse Width	100		ns
t_{DBP}	BCLK Period	100		ns
F_{BCLK}	BCLK Frequency ($1/t_{DBP}$)†		10	MHz
t_{DBL}	BCLK LO Pulse Width	40		ns
t_{DBH}	BCLK HI Pulse Width	40		ns
t_{DLS}	LRCLK Setup to BCLK	10		ns
t_{DDS}	SDATA Setup to BCLK	90		ns
t_{DDH}	SDATA Hold from BCLK	15		ns
t_{SFPW}	SFCLK HI Pulse Width	100		ns
t_{SFSU}	VBIT, UBIT, CSBIT, PARITY, ERROR Setup to SFCLK	40		ns
t_{CSPW}	CSCLK HI Pulse Width	100		ns
t_{CSSU}	CA, CB, CC, CD, CE, CON/$\overline{\text{PRO}}$ Setup to CSCLK	40		ns
t_{LRSU}	CSLR Setup to CSCLK	20		ns

POWER

		Min	Typ	Max	Units
Supplies					
	Voltage, DV_{DD}	2.7		5.5	V
	Operational Current, I_{DD} (DV_{DD} = +5.0 V)		TBD	TBD	mA
	Operational Current, I_{DD} (DV_{DD} = +3.0 V)		TBD	TBD	mA
	Power-Down Current, I_{DD} (DV_{DD} = +5.0 V)		TBD	TBD	mA
	Power-Down Current, I_{DD} (DV_{DD} = +3.0 V)		TBD	TBD	mA
Dissipation†					
	Operational (DV_{DD} = +5.0 V)		TBD	TBD	mW
	Operational (DV_{DD} = +3.0 V)		TBD	TBD	mW
	Power-Down (DV_{DD} = +5.0 V)		TBD	TBD	mW
	Power-Down (DV_{DD} = +3.0 V)		TBD	TBD	mW

TEMPERATURE RANGE

	Min	Typ	Max	Units
Specifications Guaranteed		+25		°C
Operation Guaranteed	0		+70	°C
Storage	–60		+100	°C

ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units
DV_{DD} to DGND	–0.3	7.0	V
DC Input Voltage	–0.3	DV_{DD} + 0.3	V
Latch-Up Trigger Current	–1000	+1000	mA
Soldering		+300	°C
		10	sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

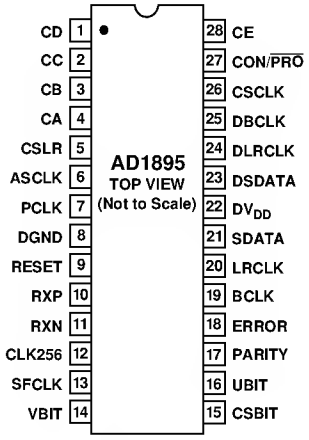
†Guaranteed, Not Tested

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1895JRS	0°C to +70°C	SSOP	RS-28

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1895 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD1895 PIN LIST

Biphase-Mark Serial Inputs

Pin Name	SSOP	I/O	Description
RXP	10	I	Positive differential biphase-mark serial digital audio receiver input. 20 mV hysteresis.
RXN	11	I	Negative differential biphase-mark serial digital audio receiver input. 20 mV hysteresis.

Decoded Channel Status Outputs

Pin Name	SSOP	I/O	Description
CA	4	O	In consumer or professional mode, CA is the inverse of channel status bit 1, byte 0 ($\overline{C1}$, audio/non-audio). CA = 0 indicates non-audio, CA = 1 indicates audio. CA = 0 can be used to indicate AC-3 encoded data.
CB	3	O	In consumer mode, CB is the inverse of channel status bit 2, byte 0 ($\overline{C2}$, copy/copyright). CB = 0 indicates copy permitted/copyright not asserted, CB = 1 indicates copy inhibited/copyright asserted. In professional mode, CB is defined as the least significant bit of the two bits which encode the emphasis status of the audio material.
CC	2	O	In consumer mode, CC is the inverse channel status bit 3, byte 0 ($\overline{C3}$, pre-emphasis). CC = 0 indicates that the audio material has been pre-emphasized, CC = 1 indicates that the audio material has not been pre-emphasized. In professional mode, CC is defined as the most significant bit of the two bits which encode the emphasis status of the audio material. Table I indicates the professional mode emphasis encoding.
CD	1	O	In consumer mode, CD indicates that the audio material is original over all category codes. The state of this bit is affected by both the generation status "L" bit (channel status bit 15, byte 1) and the category code (channel status bits 8 through 14, byte 1), since the definition of the L bit is reversed for three of the category codes (001XXXX, 0111XXX, and 100XXXX). CD = 0 indicates that the audio material is original. CD = 1 indicates that the audio material is a copy (first generation or higher). In professional mode, CD is the inverse of channel status bit 9, byte 1. CD provides some information about channel mode. See below for additional details.
CE	28	O	In consumer mode, CE indicates the so-called "ignorant" category codes of "general" (0000 000) and "A/D converter without copyright information" (0110 000). CE = 0 indicates that the audio material is encoded using an ignorant category code. CE = 1 indicates that the audio material is not encoded using an ignorant category code. This status output can be used in conjunction with the CD output to implement SCMS copy protection. See below for additional details. In professional mode, CE indicates a Cyclic Redundancy Code (CRC) check error. CE = 0 indicates that the calculated CRC value does not match the received CRC value. CE = 1 indicates that the calculated CRC value does match the received CRC value. CE may be used to enable the display of the CA through CD states. If CE = 0, then CA through CD may be considered to be in error, and their display should not be updated.

Table I. Professional Mode Emphasis Encoding

AD1895 Outputs		Byte 0 Channel Status Bits			Status
CC	CB	C2	C3	C4	
1	1	0	0	0	Emphasis not indicated. Receiver defaults to no emphasis with manual override enabled.
1	0	1	0	0	None. Receiver manual override disabled.
0	1	1	1	0	50 μs/15 μs. Receiver manual override disabled.
0	0	1	1	1	CCITT J.17. Receiver manual override disabled.

			Table II summaries the function of the CA through CE pins, depending on the operating mode (professional or consumer).

Table II. Decoded Channel Status Output Functions

Pin	Consumer	Professional
CA	0 = Audio, 1 = Non-Audio	0 = Audio, 1 = Non-Audio
CB	0 = Copy Permitted, 1 = Copy Inhibited	Pre-emphasis Encoding
CC	0 = Pre-emphasis, 1 = No Pre-emphasis	Pre-emphasis Encoding
CD	0 = Original, 1 = Copy	Inverse of Channel Status Bit 9
CE	0 = Ignorant Category, 1 = Not Ignorant	0 = C.S. CRC Error, 1 = No C.S. CRC Error

CON/$\overline{\text{PRO}}$	27	O	CON/$\overline{\text{PRO}}$ is defined as the inverse of channel status bit 0, byte 0 (C0, pro/consumer). CON/$\overline{\text{PRO}}$ = 0 indicates professional mode. CON/$\overline{\text{PRO}}$ = 1 indicates consumer mode. The state of this pin internally determines the consumer/pro mode of the CA, CB, CC, CD and CE pins.
CSCLK	26	O	Channel Status Clock. Active HI (rising edge active). Outputs a pulse every 192 frames, at the start of the channel status block. Use this clock to latch the CA through CE and CON/$\overline{\text{PRO}}$ output channel status signals. See Figure 22 for timing.

Channel Status Input Control Signal

Pin Name	SSOP	I/O	Description
CSLR	5	I	This input determines whether CA through CE and CON/$\overline{\text{PRO}}$ output channel status information from the left channel (subframe A) or the right channel (subframe B). CSLR = 0 selects the left channel. CSLR = 1 selects the right channel.

Direct Output Signals (Jittered)

Pin Name	SSOP	I/O	Description
DLRCLK	24	O	Left/$\overline{\text{right}}$ clock derived directly from the biphase-mark input stream. HI for the left channel, LO for the right channel. This is a jittered output clock! Use this output to feed one input of the phase detector of the external analog phase lock loop. See Figure 20 for timing.
DBCLK	25	O	Bit clock derived directly from the biphase-mark input stream. Falling edge active (i.e., DSDATA is valid on the falling edge of DBCLK). This is a jittered output clock! This clock is gated to produce 24 pulses per sample (left or right) aligned with the data. See Figure 20 for timing.
DSDATA	23	O	Serial data derived directly from the biphase-mark input stream. This is a jittered signal! All 24 bits are output (20 bits of audio data plus 4 bits of auxiliary data), LSB first. Unlike the SDATA output (Pin 21), this output does not hold the last valid sample when the current sample is invalid. See Figure 20 for timing.

Digital Audio Output Signals (I^2S-Compatible)

Pin Name	SSOP	I/O	Description
LRCLK	20	O	Left/$\overline{\text{right}}$ clock for the output serial digital audio stream. HI for the left channel, LO for the right channel. LRCLK is the external analog PLL voltage controlled oscillator (VCO) output divided down by 512. Use this low jitter output clock to feed the second input of the phase detector of the external analog phase lock loop. See Figure 18 for timing.
BCLK	19	O	Bit clock for the output serial digital audio stream. Serial data is valid on the rising edge of BCLK. There are 32 bit clock periods for the left sample, and 32 bit clock periods for the right channel (i.e., the bit clock frequency is 64 × FS). BCLK is the external analog PLL VCO output divided down by 8. Use this signal to clock the audio data into downstream DACs, sample rate converters or DSPs. See Figure 18 for timing.
SDATA	21	O	Serial Audio Data. All 24 bits are output (20 bits audio data plus 4 bits of auxiliary data), MSB first. When the current sample is invalid, the last valid sample is repeated. See Figure 18 for timing.

Clock Input Signals

Pin Name	SSOP	I/O	Description
ASCLK	6	I	Under normal conditions (when using the AD1895 with an external analog PLL), ASCLK should be connected to the PLL's VCO output, which runs at 512 × FS. If an external PLL is not used (not normal configuration), ASCLK must be fed with an asynchronous clock at a frequency above 20 MHz.
PCLK	7	I	Under normal conditions (when using the AD1895 with an external analog PLL), PCLK should be connected to the PLL's VCO output, which runs at 512 × FS. If an external PLL is not used (not normal configuration), PCLK should be grounded, which has the effect of shutting off the digital audio output signals (LRCLK, BCLK and SDATA) as well.

Clock Output Signals

Pin Name	SSOP	I/O	Description
CLK256	12	O	CLK256 is an output clock at a frequency of 256 times the recovered sample frequency (i.e., LRCLK). Useful for downstream digital audio devices such as DACs, sample rate converters, DSPs and digital audio transmitters.

Error Output Signals

Pin Name	SSOP	I/O	Description
ERROR	18	O	The ERROR pin is HI when there is no biphase-mark signal present, or when the frequency of the ASCLK input (Pin 6) frequency is too low for the AD1895 to function properly. The ERROR bit can be clocked using the SFCLK signal (Pin 13). NOTE: When no biphase-mark signal is present or the ASCLK input frequency is too low, the DLRCLK (Pin 24) signal that the external PLL locks to is changed to a divided-down version of the PLL clock. This divide ratio is set such that the PLL should "park" at the highest frequency possible. This is important to prevent "latch-up" where the clock input signal frequency is too low to be able to decode the left/right clock from the biphase-mark stream, which makes the PLL go to an even lower frequency, and then the system is "stuck" and unable to recover.
PARITY	17	O	PARITY is the computed parity status from the biphase-mark stream. Even parity is computed and compared against the incoming parity bit, which occurs on each subframe. The parity output (error = HI or no error = LO) is held for the entire subframe, until the next parity bit arrives. This output is not affected by the subframe select pin (CSLR, Pin 5); the parity check is done on each subframe. The PARITY bit can be clocked using the SFCLK signal (Pin 13).

Subframe Status Output Signals

Pin Name	SSOP	I/O	Description
VBIT	14	O	VBIT is the validity bit from the biphase-mark stream, fed out serially, valid on the rising edge of the SFCLK signal (Pin 13). VBIT = 0 indicates that the current audio sample is suitable for further processing (i.e., valid). VBIT = 1 indicates that the current audio sample is not suitable for further processing (i.e., not valid). Not affected by the subframe select pin (CSLR, Pin 5). Changes at the subframe rate (two times the sample rate).
UBIT	16	O	UBIT is the user bit from the biphase-mark stream, fed out serially, valid on the rising edge of the SFCLK signal (Pin 13). Not affected by the subframe select pin (CSLR, Pin 5). Changes at the subframe rate (two times the sample rate).
CSBIT	15	O	CSBIT is the channel status bit from the biphase-mark stream, fed out serially, valid on the rising edge of the SFCLK signal (Pin 13). Not affected by the subframe select pin (CSLR, Pin 5). Changes at the subframe rate (two times the sample rate).
SFCLK	13	O	This clock is used to clock the VBIT, UBIT, CSBIT, PARITY and ERROR output status signals. Active HI (rising edge active), see Figure 21 for timing. It is a pulse at the subframe rate (two times the sample rate).

Reset

Pin Name	SSOP	I/O	Description
RESET	9	I	RESET is an active HI signal which, when asserted, clears all on-chip registers on the AD1895 to their default state.

Power Supply Connections

Pin Name	SSOP	I/O	Description
DV_{DD}		22	Digital Supply. +3 V to +5 V nominal supply voltage.
DGND		8	Digital Ground. +0 V nominal supply connection.

SERIAL DIGITAL AUDIO TRANSMISSION STANDARDS

The AD1895 can receive S/PDIF [Sony/Philips Digital Interface Format], AES/EBU [Audio Engineering Society/European Broadcasting Union, as known as AES3-1992], IEC-958 [International Electrotechnical Commission] and CP-340 (EIAJ [Electronic Industry Association of Japan] CP-1201) serial streams. S/PDIF is a consumer audio standard and AES/EBU is a professional audio standard; IEC-958 and CP-340 have both consumer and professional definitions.

All of these digital audio serial communication schemes encode audio data and audio control information using the biphase-mark method. This encoding method minimizes the dc content of the transmitted signal, and allows the receiver to decode clock information from the transmitted signal. As can be seen from Figure 1, 1s in the original data end up with midcell transitions in the biphase-mark encoded data, while 0s in the original data do not. Note that the biphase-mark encoded data always has a transition between bit boundaries.

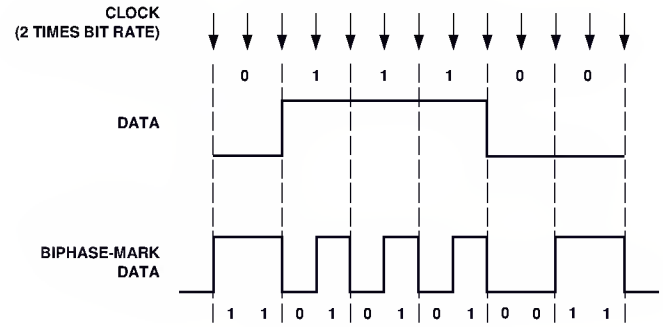


Figure 1. Biphase-Mark Encoding

Digital audio communication schemes use "preambles" to distinguish between channels (called "subframes") and between longer term control information blocks (called "frames"). Preambles are particular biphase-mark patterns which contain encoding violations which allow the receiver to uniquely recognize them. These patterns and their relationship to frames and subframes are shown in Figures 2 and 3.

	BIPHASE PATTERNS	CHANNEL
X	11100010 OR 00011101	LEFT
Y	11100100 OR 00011011	RIGHT
Z	11101000 OR 00010111	LEFT AND C.S. BLOCK START

Figure 2. Biphase-Mark Encoded Preambles

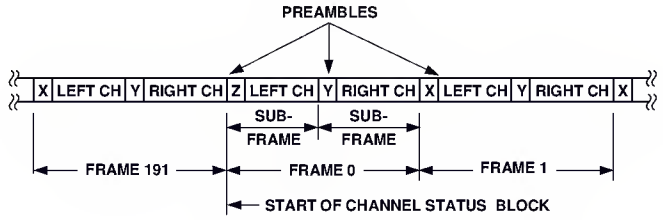


Figure 3. Preambles, Frames and Subframes

The biphase-mark encoding violations are shown in Figure 4. Note that all three preambles include encoding violations. Ordinarily, the biphase-mark encoding method results in a polarity transition between bit boundaries.

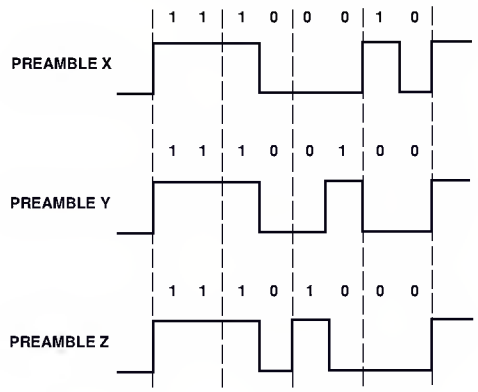


Figure 4. Preambles

As noted above, these serial digital audio communication schemes are organized using a frame and subframe construction. There are two subframes per frame (ordinarily the left and right channel). Each subframe includes the appropriate four-bit preamble, four bits of "auxiliary" (aux) data, 20 bits of audio data (LSB first), a "validity" bit, a "user" data bit, a channel status bit, and an even parity bit. The channel status bits and the user bits accumulate over many frames to convey control information. The channel status bits accumulate over a 192 frame period (called a channel status block). The user bits accumulate over 1176 frames when the interconnect is implementing the so-called "subcode" scheme (EIAJ CP-2401). The organization of the channel status block, frames and subframes is shown in Figure 5.

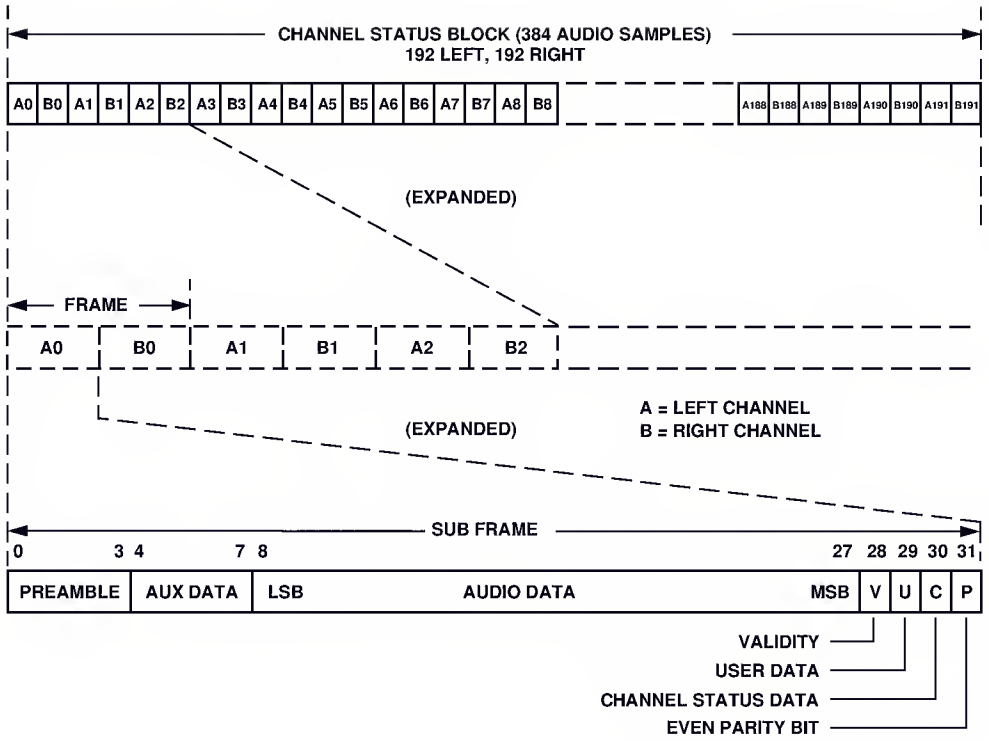


Figure 5. Block, Frame and Subframe Organization

As noted above, the channel status bit from each subframe accumulates over a 192 subframe period. The standards allow for the channel status bit in each subframe to be independent, but ordinarily the channel status bit in the two subframes of each frame are the same. The channel status bit are defined differently for the consumer audio standards and the professional audio standards. The 192-channel status bit is organized into 24 bytes, and has the interpretations shown in Figures 6 through 16.

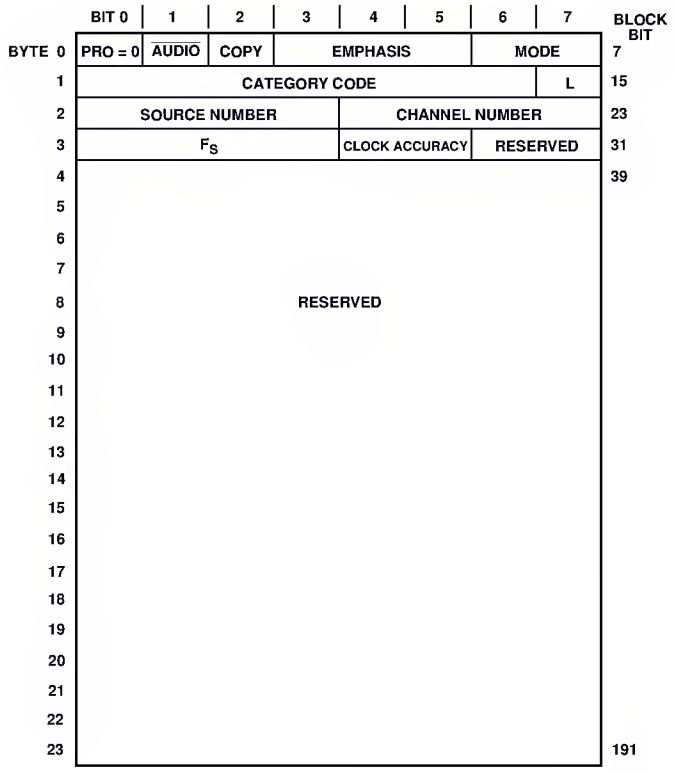


Figure 6. Consumer Channel Status Block Structure

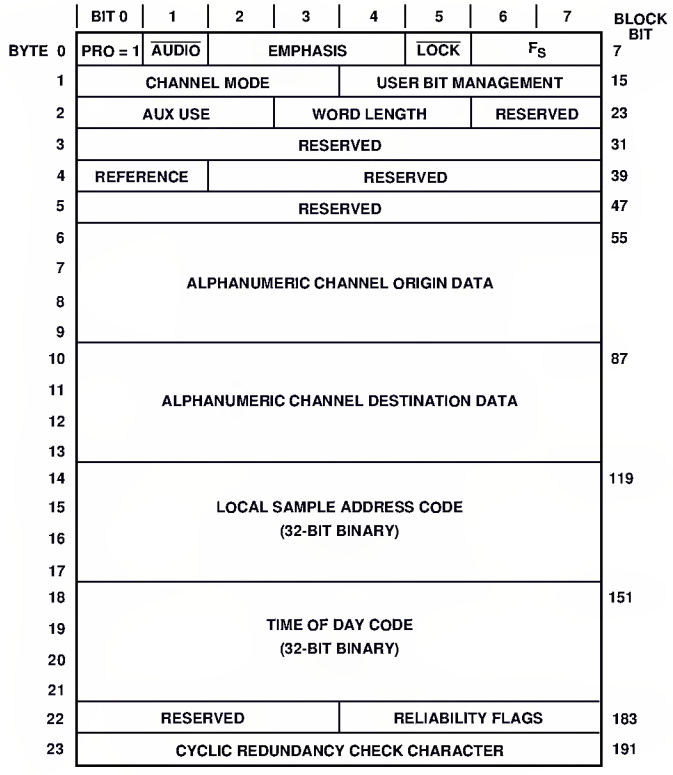


Figure 7. Professional Channel Status Block Structure

BYTE 0	
BIT 0	PRO = 0 (CONSUMER)
0	CONSUMER USE OF CHANNEL STATUS BLOCK.
1	PROFESSIONAL USE OF CHANNEL STATUS BLOCK.
BIT 1	$\overline{\text{AUDIO}}$
0	DIGITAL AUDIO.
1	NON-AUDIO. CAN BE USED TO INDICATE AC-3 DATA.
BIT 2	COPY/COPYRIGHT.
0	COPY INHIBITED/COPYRIGHT ASSERTED.
1	COPY PERMITTED/COPYRIGHT NOT ASSERTED.
BITS 3 4 5	PRE-EMPHASIS – IF BIT 1 = 0 (DIGITAL AUDIO)
0 0 0	NONE – 2 CHANNEL AUDIO.
1 0 0	50/15 µs – 2 CHANNEL AUDIO.
0 1 0	RESERVED – 2 CHANNEL AUDIO.
1 1 0	RESERVED – 2 CHANNEL AUDIO.
X X 1	RESERVED – 4 CHANNEL AUDIO.
BITS 3 4 5	IF BIT 1 = 1 (NON-AUDIO)
0 0 0	DIGITAL DATA.
X X X	ALL OTHER STATES OF BITS 3–5 ARE RESERVED.
BITS 6 7	MODE
0 0	MODE 0 (DEFINES BYTES 1–3)
X X	ALL OTHER STATES OF BITS 6–7 ARE RESERVED.

Figure 8. Consumer Channel Status Byte 0

BYTE 1		
BITS 0 1 2 3	4 5 6	CATEGORY CODE
0 0 0 0	0 0 0	GENERAL. "IGNORANT" CATEGORY CODE.
	0 0 1	EXPERIMENTAL.
	X X X	RESERVED.
0 0 0 1	X X X	SOLID STATE MEMORY.
0 0 1		BROADCAST RECEPTION OF DIGITAL AUDIO. L BIT DEFINITION REVERSED.
	0 0 0 0	JAPAN
	0 0 1 1	UNITED STATES.
	1 0 0 0	EUROPE.
	0 0 0 1	ELECTRONIC SOFTWARE DELIVERY.
	X X X X	ALL OTHER STATES ARE RESERVED.
0 1 0		DIGITAL/DIGITAL CONVERTERS
	0 0 0 0	PCM ENCODER/DECODER.
	0 0 1 0	DIGITAL SOUND SAMPLER.
	0 1 0 0	DIGITAL SIGNAL MIXER.
	1 1 0 0	SAMPLE RATE CONVERTER.
	X X X X	ALL OTHER STATES ARE RESERVED.
0 1 1 0		A/D CONVERTERS
	0 0 0	A/D CONVERTER WITHOUT COPY PROTECTION INFO "IGNORANT" CATEGORY CODE.
	1 0 0	A/D CONVERTER WITH COPY PROTECTION INFO (USING COPY AND L BITS).
0 1 1 1	X X X	BROADCAST RECEPTION OF DIGITAL AUDIO. L BIT DEFINITION REVERSED.
1 0 0		LASER OPTICAL. L BIT DEFINITION REVERSED.
	0 0 0 0	CD – COMPATIBLE WITH IEC-908.
	1 0 0 0	CD – NOT COMPATIBLE WITH IEC-908. (MAGNETO-OPTICAL).
	1 0 0 1	MD – MINIDISC.
	X X X X	ALL OTHER STATES ARE RESERVED.
1 0 1		MUSICAL INSTRUMENTS, MICS, ETC.
	0 0 0 0	SYNTHESIZER.
	1 0 0 0	MICROPHONE.
	X X X X	ALL OTHER STATES ARE RESERVED.
1 1 0		MAGNETIC TAPE OR DISK
	0 0 0 0	DAT – DIGITAL AUDIO TAPE.
	1 0 0 0	VIDEO TAPE RECORDER WITH DIGITAL AUDIO.
	0 0 0 1	DCC – DIGITAL COMPACT CASSETTE
	X X X X	ALL OTHER STATES ARE RESERVED.
1 1 1	X X X X	RESERVED.
BIT 7		L: GENERATION STATUS
		ONLY CATEGORY CODES: 1 0 0 X X X X, 0 0 1 X X X X, 0 1 1 1 X X X
0		ORIGINAL/COMMERCIALLY PRE-RECORDED DATA.
1		NO INDICATION /1ST GENERATION OR HIGHER.
		ALL OTHER CATEGORY CODES
0		NO INDICATION /1ST GENERATION OR HIGHER.
1		ORIGINAL/COMMERCIALLY PRE-RECORDED DATA.

Figure 9. Consumer Channel Status Byte 1

BYTE 2	
BITS 0 1 2 3	SOURCE NUMBER
0 0 0 0	UNSPECIFIED.
1 0 0 0	1
0 1 0 0	2
1 1 0 0	3
0 0 1 0	4 TO
0 1 1 1	14 (BINARY – BIT 0 IS LSB, BIT 3 IS MSB)
1 1 1 1	15
BITS 4 5 6 7	CHANNEL NUMBER
0 0 0 0	UNSPECIFIED.
1 0 0 0	A (LEFT IN 2 CHANNEL FORMAT)
0 1 0 0	B (RIGHT IN 2 CHANNEL FORMAT)
1 1 0 0	C TO
0 1 1 1	N (BINARY – BIT 4 IS LSB, BIT 7 IS MSB)
1 1 1 1	O

Figure 10. Consumer Channel Status Byte 2

BYTE 3	
BITS 0 1 2 3	F_S: SAMPLE FREQUENCY
0 0 0 0	44.1 kHz.
0 1 0 0	48 kHz.
1 1 0 0	32 kHz.
X X X X	ALL OTHER STATES OF BIT 0–3 ARE RESERVED.
BITS 4 5	CLOCK ACCURACY
0 0	LEVEL II, ±1000 ppm (DEFAULT).
0 1	LEVEL III, VARIABLE PITCH.
1 0	LEVEL I, ±50 ppm – HIGH ACCURACY.
1 1	RESERVED.
BITS 6 7	
X X	RESERVED.

BYTES 4–23
RESERVED

Figure 11. Consumer Channel Status Bytes 3 through 23

BYTE 0	
BIT 0	PRO = 1
0	CONSUMER USE OF CHANNEL STATUS BLOCK.
1	PROFESSIONAL USE OF CHANNEL STATUS BLOCK.
BIT 1	$\overline{\text{AUDIO}}$
0	NORMAL AUDIO.
1	NON-AUDIO. CAN BE USED TO INDICATE AC-3 DATA.
BITS 2 3 4	ENCODED AUDIO SIGNAL EMPHASIS
0 0 0	EMPHASIS NOT INDICATED. RECEIVER DEFAULTS TO NO EMPHASIS WITH MANUAL OVERRIDE ENABLED.
1 0 0	NONE. RECEIVER MANUAL OVERRIDE DISABLED.
1 1 0	50/15 µs. RECEIVER MANUAL OVERRIDE DISABLED.
1 1 0	CCITT J.17. RECEIVER MANUAL OVERRIDE DISABLED.
X X X	ALL OTHER STATES OF BITS 2–4 ARE RESERVED.
BIT 5	$\overline{\text{LOCK}}$: SOURCE SAMPLE FREQUENCY
0	LOCKED–DEFAULT.
1	UNLOCKED.
BITS 6 7	F_S: SAMPLE FREQUENCY
0 0	SAMPLE FREQUENCY NOT INDICATED. RECEIVER DEFAULTS TO 48 kHz AND MANUAL OVERRIDE OR AUTO SET ENABLED.
0 1	48 kHz. MANUAL OVERRIDE OR AUTO SET DISABLED.
1 0	44.1 kHz. MANUAL OVERRIDE OR AUTO SET DISABLED.
1 1	32 kHz. MANUAL OVERRIDE OR AUTO SET DISABLED.

BYTE 1	
BITS 0 1 2 3	CHANNEL MODE
0 0 0 0	MODE NOT INDICATED. RECEIVER DEFAULTS TO 2-CHANNEL MODE. MANUAL OVERRIDE ENABLED.
0 0 0 1	TWO CHANNELS. MANUAL OVERRIDE DISABLED.
0 0 1 0	SINGLE CHANNEL. MANUAL OVERRIDE DISABLED.
0 0 1 1	PRIMARY/SECONDARY (CH. A IS PRIMARY). MANUAL OVERRIDE DISABLED.
0 1 0 0	STEREOPHONIC (CH. A IS LEFT). MANUAL OVERRIDE DISABLED.
0 1 0 1	RESERVED FOR USED DEFINED APPLICATIONS.
0 1 1 0	RESERVED FOR USED DEFINED APPLICATIONS.
1 1 1 1	VECTOR TO BYTE 3. RESERVED.
X X X X	ALL OTHER STATES OF BITS 0–3 ARE RESERVED.
BITS 4 5 6 7	USER BIT MANAGEMENT
0 0 0 0	DEFAULT. NO USER INFORMATION INDICATED.
0 0 0 1	192 BIT BLOCK STRUCTURE. PREAMBLE 'Z' STARTS BLOCK.
0 0 1 0	RESERVED.
0 0 1 1	USER DEFINED APPLICATION.
X X X X	ALL OTHER STATES OF BITS 4–7 ARE RESERVED.

Figure 12. Professional Channel Status Bytes 0 and 1

BYTE 2			
BITS 0 1 2	AUX: USE OF AUXILIARY SAMPLE BITS		
0 0 0	NOT DEFINED. MAXIMUM AUDIO WORD LENGTH IS 20 BITS.		
0 0 1	USED FOR MAIN AUDIO. MAXIMUM AUDIO WORD LENGTH IS 24 BITS.		
0 1 0	SINGLE COORDINATION SIGNAL. MAXIMUM AUDIO WORD LENGTH IS 20 BITS.		
0 1 1	USER DEFINED APPLICATION.		
X X X	ALL OTHER STATES OF BITS 0–2 ARE RESERVED.		
BITS 3 4 5	SOURCE WORD LENGTH		
	MAX AUDIO 24 BITS	MAX AUDIO 20 BITS	
0 0 0	NOT INDICATED	NOT INDICATED (DEFAULT)	
0 0 1	23 BITS	19 BITS	
0 1 0	22 BITS	18 BITS	
0 1 1	21 BITS	17 BITS	
1 0 0	20 BITS	16 BITS	
1 0 0	24 BITS	20 BITS	
X X X	ALL OTHER STATES OF BITS 3–5 ARE RESERVED.		
BITS 6 7			
X X	RESERVED.		

Figure 13. Professional Channel Status Byte 2

BYTE 3	
BITS 0–7	VECTORED TARGET BYTE
X X X X X X X X	RESERVED.

BYTE 4	
BITS 0 1	DIGITAL AUDIO REFERENCE SIGNAL PER AES11-1990
0 0	NOT REFERENCE SIGNAL (DEFAULT).
0 1	GRADE 1 REFERENCE SIGNAL.
1 0	GRADE 2 REFERENCE SIGNAL.
1 1	RESERVED.
BITS 2–7	
X X X X X X	RESERVED.

BYTE 5	
BITS 0–7	
X X X X X X X X	RESERVED.

Figure 14. Professional Channel Status Bytes 3 through 5

BYTES 6–9
ALPHANUMERIC CHANNEL ORIGIN DATA.
7-BIT ISO 646 (ASCII) DATA WITH ODD PARITY BIT. FIRST CHARACTER IN MESSAGE IS BYTE 6. LSBs ARE TRANSMITTED FIRST.

BYTES 10–13
ALPHANUMERIC CHANNEL ORIGIN DATA.
7-BIT ISO 646 (ASCII) DATA WITH ODD PARITY BIT. FIRST CHARACTER IN MESSAGE IS BYTE 10. LSBs ARE TRANSMITTED FIRST.

BYTES 14–17
LOCAL SAMPLE ADDRESS CODE (32-BIT BINARY)
VALUE IS OF FIRST SAMPLE OF CURRENT BLOCK. LSBs ARE TRANSMITTED FIRST.

BYTES 18–21
TIME-OF-DAY SAMPLE ADDRESS CODE (32-BIT BINARY).
VALUE IS OF FIRST SAMPLE OF CURRENT BLOCK. LSBs ARE TRANSMITTED FIRST.

Figure 15. Professional Channel Status Bytes 6 through 21

BYTE 22	
BITS 0 1 2 3	
X X X X	RESERVED.
BIT 4	CHANNEL STATUS BYTES 0 TO 5
0	RELIABLE.
1	UNRELIABLE.
BIT 5	CHANNEL STATUS BYTES 6 TO 13
0	RELIABLE.
1	UNRELIABLE.
BIT 6	CHANNEL STATUS BYTES 14 TO 17
0	RELIABLE.
1	UNRELIABLE.
BIT 7	CHANNEL STATUS BYTES 18 TO 21
0	RELIABLE.
1	UNRELIABLE.

BYTE 23
CRCC: CYCLIC REDUNDANCY CHECK CHARACTER.
CRCC FOR CHANNEL STATUS DATA BLOCK THAT USES BYTES 0 TO 22 INCLUSIVE. GENERATING POLYNOMIAL IS: $G(x) = x^8 + x^4 + x^3 + x^2 + 1$ WITH AN INITIAL STATE OF ALL ONES.

Figure 16. Professional Channel Status Bytes 22 and 23

OPERATING ISSUES

Non-PLL Mode

It is possible to operate the AD1895 without an external PLL. The normally low jitter I²S interface will have jitter, which may be ignored if the AD1895 is used with an asynchronous sample rate converter (ASRC) such as the AD1890 or AD1893.

The serial output may be used provided that there is some external logic which obeys the following constraints. On either transition of the DLRCLK output signal (Pin 24), the logic must supply 256 pulses to the PCLK input (Pin 7) at a frequency high enough to insure that all 256 pulses have been applied before the next DLRCLK transition. After the 256 pulses have been applied, the logic must stop and wait for the next DLRCLK transition. This scheme has the advantage that the "sample-repeat" feature still works, and the interface (BCLK [Pin 19], LRCLK [Pin 20], and SDATA [Pin 21]) is still I²S compatible.

APPLICATION ISSUES

The recommended application circuit for the AD1895 is shown in Figure 17.

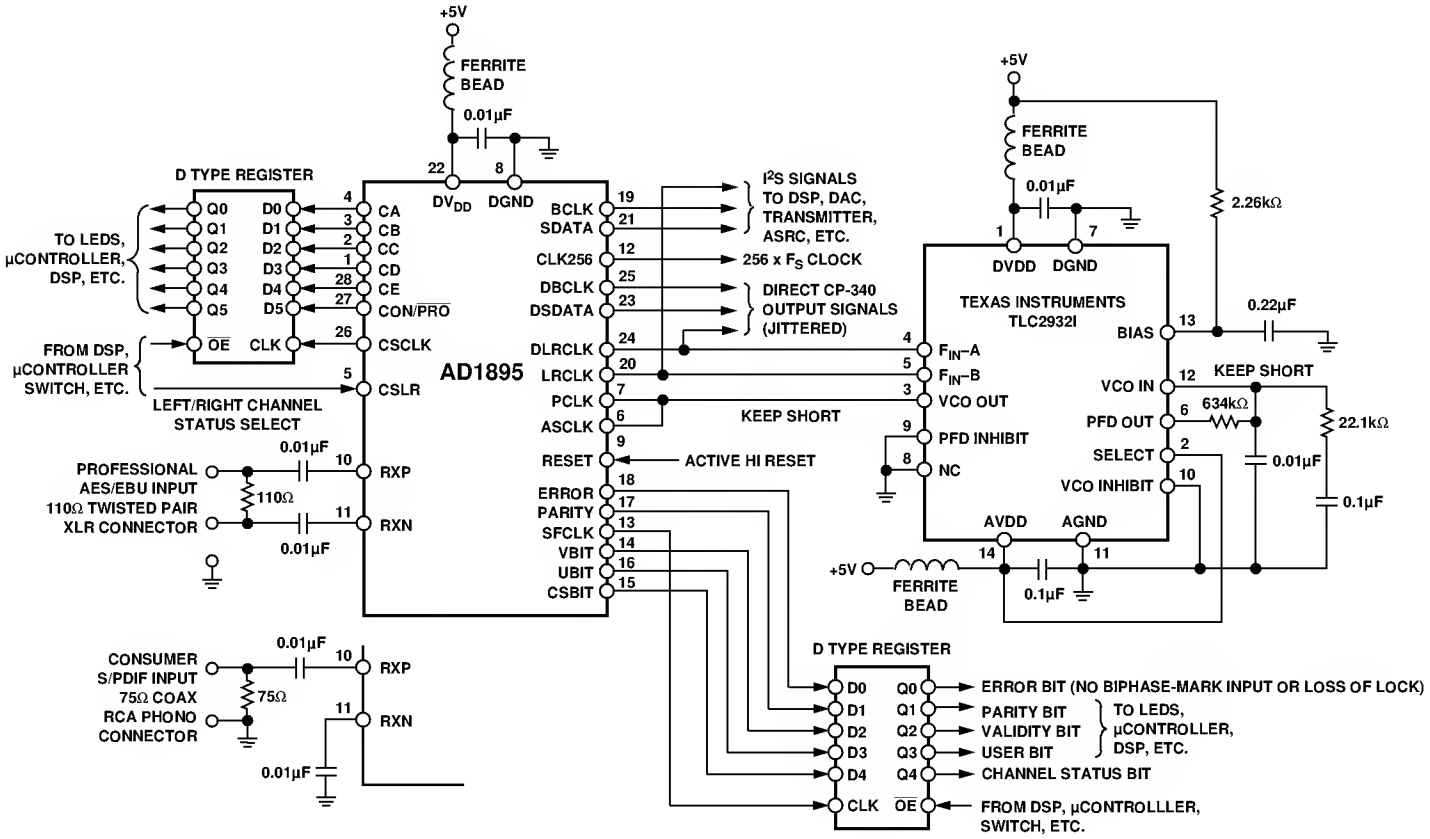


Figure 17. Recommended Application Circuit

TIMING DIAGRAMS

The AD1895 timing diagrams are shown in Figures 18 through 22.

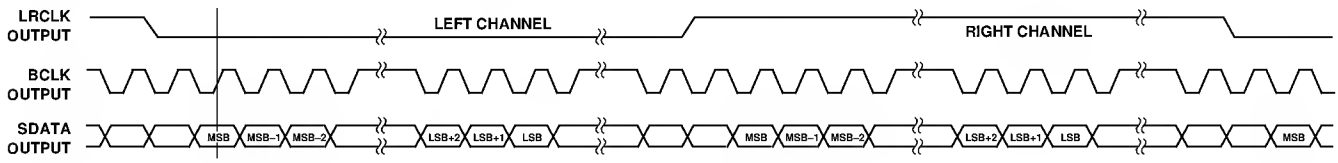


Figure 18. I²S Output Format

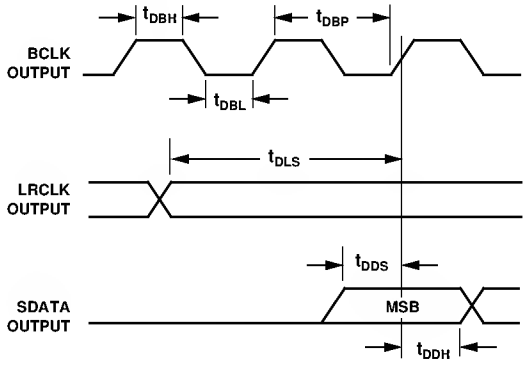


Figure 19. Serial Data Output Port Timing

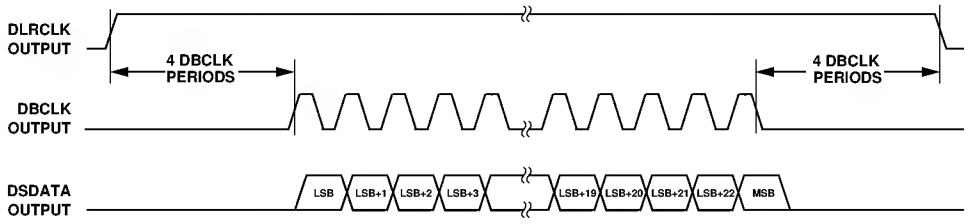


Figure 20. Direct Output Signal Timing

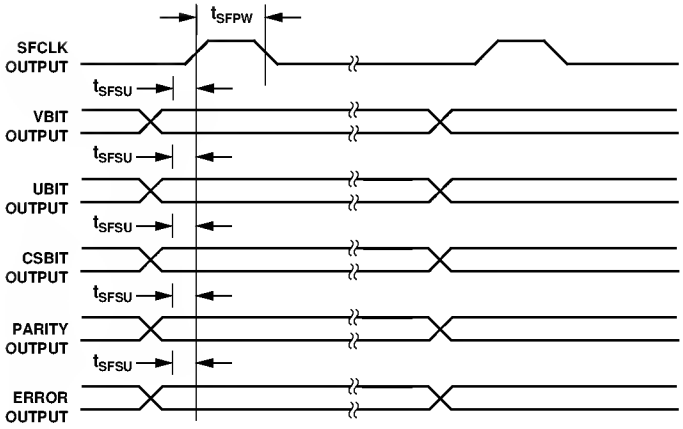


Figure 21. Subframe Status, Error and Clock Timing

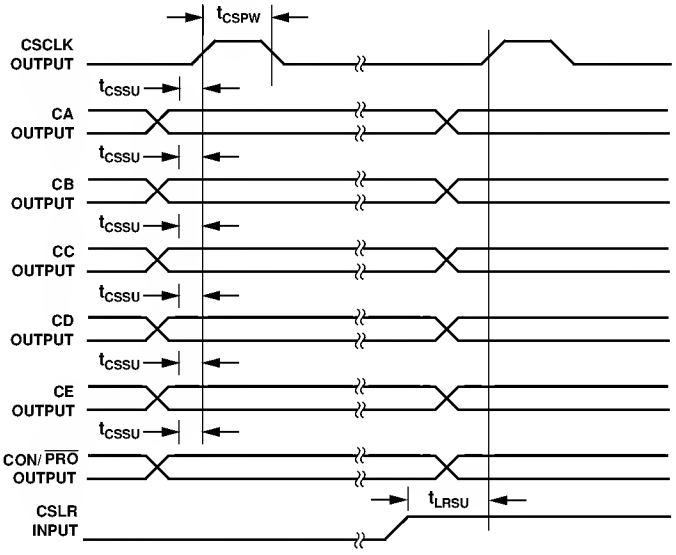


Figure 22. Channel Status and Clock Timing

TYPICAL PERFORMANCE

The typical jitter rejection performance of the AD1895 is shown in Figure 23.

Figure 23. Jitter Rejection

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead SSOP
(RS-28)